Closing Session

High Temperature Performance of 10 kV, 200 A (Pulsed) 4H-SiC PiN Rectifiers
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Electrical Activation of Implanted Phosphorus Ions in (0001)/(112 – 0)-Oriented 4H-SiC
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Selective Epitaxial Growth of Pyramidal 3C-SiC on Patterned Si Substrate
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Heteroepitaxial Growth of Defect-Free 3C-SiC on Step-Free Hexagonal (0001) SiC Mesas
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AlGaN/GaN Hetero Field Effect Transistor for a Large Current Operation
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High Temperature performance of 10 Kilovolts, 200 Amperes (Pulsed) 4H-SiC PiN Rectifiers

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SiC is a superior material system for the fabrication of ultra high voltage devices since it is capable of sustaining a very high power density, which can be switched at an extremely high speed, while operating at very high temperatures. Such diodes would be suitable for solid state power conditioning systems for high power radar, directed energy weapons, X-ray generators, electrostatic precipitators and high power LASERs. This paper reports the highest power single chip 4H-SiC PiN rectifier demonstrated to date, with a 2 MegaWatt (Pulsed) capability.

These diodes had an active metallized Anode area of approximately 0.09 cm^2 (3mm X 3mm). A high purity, 150 μm n^- epitaxial layer doped at 7E14 cm^{-3} was used in the fabrication of these rectifiers. This voltage-blocking layer was grown using a refined hot wall CVD growth reactor yielding low epi defect densities. The highly doped, 1.8 μm p+ Anode was grown epitaxially in order to obtain good carrier injection during on-state operation. To prevent premature breakdown, the voltage blocking layer was exposed using reactive ion etching, and a 400 μm wide, optimized Junction Termination Extension (JTE) was implemented using a p-type implant at the periphery of the device edge. The SiC surface at the edges were then passivated using a thick SiO_2 layer. This termination allowed a 10 kV blocking capability with a leakage current of only 20 μA for these 3mm X 3mm diodes. Measurements conducted up to 200°C and 3 kV show practically no change in the leakage current using our measurement system with a 3 μA sensitivity. Measurements at higher voltages will be presented at the conference.

The forward characteristics were found to be fairly uniform on rectifiers fabricated throughout the wafer, with most rectifiers turning on close to the built-in voltage (2.9 to 3 V) of 4H-SiC. Thereafter, these rectifiers have a much steeper I-V slope as compared to Si diodes. At room temperature, pulsed measurements using a high power curve tracer shows that the forward voltage drop was 4.5 V at 100 A/cm^2 (10 A); 7.07 V at 500 A/cm^2 (45 A); and only 12.5 V at 2200 A/cm^2 (200 A). On-state measurements conducted in the room temperature to 200°C temperature range (in 50°C intervals) show a slight reduction in on-state voltage drop from 7.2 V to 6.9 V at 50 A on this packaged device.

These rectifiers show fairly stable reverse recovery switching characteristics as the operating temperature was increased from 25°C to 200°C. A forward current of 20 A (220 A/cm^2) was switched at a reverse dI/dt of 120 A/μsec with an applied reverse voltage of 100 V. At room temperature, the peak reverse recovery current of only 8.7 A was observed and the device turned off completely within 600 nsec. This complete turn-off time increases to 1 μsec at 200°C under similar test conditions. The peak reverse recovery increases a modest 72% to 15 A between room temperature and 200°C.

Wafer maps showing the distribution of on-state voltage drop and blocking voltage show fairly good yields when a criteria of >7 kV, 4.5 V (100 A/cm^2) is used. These data and the details of high temperature measurements will be presented at the conference.

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Electrical Activation of Implanted Phosphorus Ions in (0001)/(11$\bar{2}$0)-oriented 4H-SiC

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Rutherford Backscattering and Cross-Sectional Transmission Electron Microscopy investigations conducted by Satoh and Nakaike (1st Int. Workshop on Ultra-Low Loss Power Device Technology, May 2000, Nara, Japan) revealed that implantation-induced amorphous 6H-SiC epilayers oriented in ($1\bar{1}00$)-direction could largely be recrystallized at 1500°C preserving the polytype of the underlying layer, while (0001)-oriented 6H-SiC epilayers showed a high density of extended defects even after an anneal at 1700°C.

In this study, we have performed comparative Hall effect investigations on phosphorus (P)-implanted, Si-face/a-plane ((0001)/(11$\bar{2}$0)-oriented) p-type 4H-SiC epilayers in order to examine whether the electrical activation of P donors implanted into a-plane samples is also superior to that one in samples with Si-face. We implanted two P box profiles (profile 1: T_{impl} = room temperature, depth = 1.3 µm, [P] = 10^{18} cm^{-3}, profile 2: T_{impl} = 500°C, depth = 0.8 µm, [P] = 10^{20} cm^{-3}) and performed annealings in the temperature range from 1400° to 1700°C. As an example, the temperature dependence of the free electron concentration n and of the electron Hall mobility µ for two pairs of samples oriented in (0001) (samples 1(Si)/2(Si)) and in (11$\bar{2}$0) (samples 1(a)/2(a)) direction are displayed in Figs. 1(a)/(b). Sample 1/2 was implanted with the P profile 1/2. All the samples were annealed at 1600°C. The following results are observed: (i) The electrical activation of P donors implanted into (0001)- and (11$\bar{2}$0)-oriented 4H-SiC epilayers is identical; the compensation in (0001)- oriented samples in general exceeds that one in (11$\bar{2}$0)- oriented samples (see Fig. 1(a)). (ii) P donors can completely be activated in both types of samples up to a concentration of 10^{20} cm^{-3}. (iii) The electron Hall mobility strongly differs in (0001)/(11$\bar{2}$0)-oriented 4H-SiC epilayers (see Fig. 1(b)); its ratio at room temperature is in samples #1: µ(1(a))/µ(1(Si)) ≈ 1.3 and in samples #2: µ(2(a))/ µ(2(Si)) ≈ 2.2. The physical reasons for the observed differences in the electron Hall mobility will be discussed in the paper.

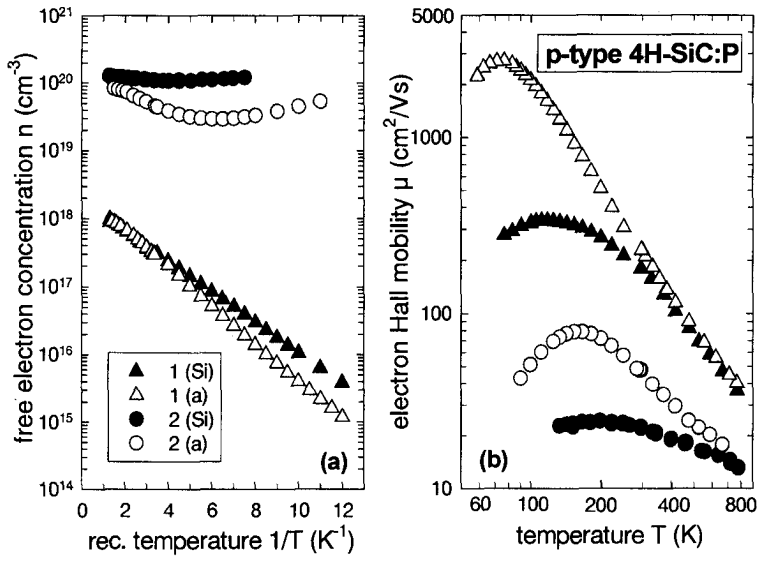

Fig.1: (a) Free electron concentration versus reciprocal temperature obtained from Hall effect investigations on P-implanted p-type 4H-SiC epilayers. (b) Hall mobility versus temperature.
Implantation:
samples 1(Si)/(a): P-box profile, depth = 1.3 µm, [P] = 10^{18} cm^{-3}, T_{impl} = room temperature.
samples 2(Si)/(a): P-box profile, depth = 0.8 µm, [P] = 10^{20} cm^{-3}. T_{impl} = 500°C.
Annealing of samples 1(Si)/(a) and 2 (Si)/(a):
T_A=1600°C, t_a=30 min.

Selective Epitaxial Growth of Pyramidal 3C-SiC on Patterned Si Substrate

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Cubic silicon carbide has been grown epitaxially on Si substrates for many years. The heteroepitaxial growth of 3C-SiC on Si has indicated the promise of high mobility devices. However, a high density of interfacial defects (misfit dislocations, voids) as well as other defects (threading dislocations, twins, stacking faults) result in the growth of lower quality material. A suitable approach towards solving this problem is the use of selective epitaxial growth on patterned silicon substrates .

Figure 1 shows the schematic of the fabrication procedure for pyramidal growth. All samples were grown by atomospheric-pressure chemical vapor deposition (APCVD) using hexamethyldisilane (HMDS). The substrates used were a (111)-oriented silicon substrates previously patterned by depositing a SiO_2 layer as the mask, followed by conventional photolithography techniques. The windows are of different shapes (square, circle, hexagonal, parallel lines) with their edges oriented mostly along the <110> directions. Thin 3C-SiC layer was grown on Si exposed through windows. After removing SiO_2 mask, patterning of the seed 3C-SiC layer was achieved by etching process to remove Si around thin 3C-SiC layer. The regrowth was carried out at the growth temperature of 1350°C. As a result of regrowth, selective growth of 3C-SiC pyramid with three facets was observed as shown in Figure 2. This approach prevents the propagation of threading dislocations originating from the 3C-SiC/Si interfaces. Therefore, lateral growth of a 3C-SiC layer until coalescence results in a 3C-SiC layer of low defect-density material. The triangular pyramids were formed on the seed 3C-SiC of different shapes (square, circle, hexagonal) without the shape of parallel lines. This indicates that the facets of each triangular pyramid do not depend on shape, wide and periodicity of the seed 3C-SiC. The air-gap was observed under the free-standing laterally grown 3C-SiC in the cross-sectional SEM.

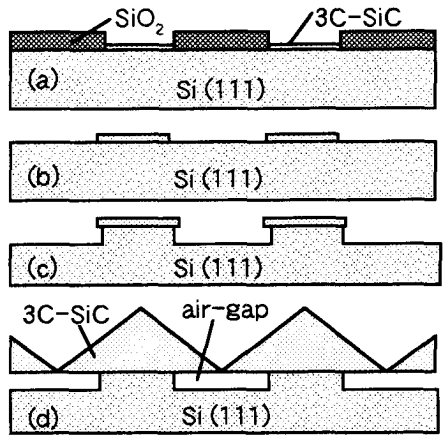

Fig. 1. Schematic of the procedure for pyramidal growth. (a) CVD of thin 3C-SiC layer at window, (b) wet etching of SiO_2 mask, (c) dry etching of Si, and (d) regrowth of 3C-SiC

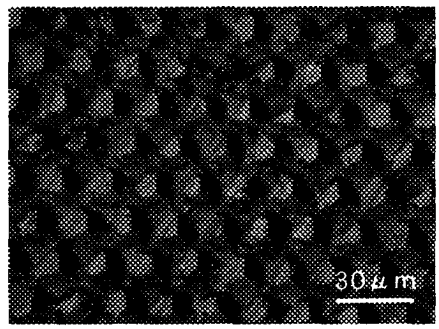

Fig. 2. Nomarski image of a triangular pyramid of 3C-SiC grown selectively by CVD.

Heteroepitaxial Growth of Defect-Free 3C-SiC on Step-Free Hexagonal (0001) SiC Mesas

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Abstract: Previous efforts to grow 3C-SiC heteroepitaxial films on Si and α-SiC substrates all yielded films containing extended defects such as double-positioning boundaries (DPB's) and/or stacking faults (SF's), leading to poor electrical performance of devices fabricated in these films. The formation of SiC mesa surfaces as large 0.2 x 0.2 mm completely free of even a single atomic step was recently reported [1]. As described in [1], these surfaces are produced on 4H- or 6H-SiC wafers (on-axis) by first dry etching trench patterns into the wafer surface to form an array of isolated growth mesas. Pure stepflow epitaxial growth, carried out under conditions that suppress 2D terrace nucleation, is then used to grow all initial surface steps on top of each mesa over to the edge of the mesa, leaving behind a top mesa surface completely free of atomic steps. However as reported in [1], mesas that initially contain screw dislocation defects cannot be flattened due to the continual spiral of new growth steps that emanate from screw dislocations during epitaxial growth.

The heteroepitaxial growth of 3C-SiC films completely free of DPB's and SF's has now been achieved at NASA Glenn on step-free 4H/6H-SiC mesas. In the absence of steps that provide a template for maintaining hexagonal substrate polytype during homoepitaxial growth, a single variant of the 3C-SiC polytype can be controllably nucleated and grown without any extended crystal defects on the step-free (0001) basal plane surface. Our experiments confirm that such defect-free growth is not possible without a step-free surface, as the presence of any steps on the nucleation surface produces disorder (i.e., extended defects) in 3C-SiC heteroepitaxial films grown thereon [2]. In particular, SF and DPB defects are observed on 3C-SiC films grown on 4H-SiC substrate mesas that could not be rendered step-free prior to 3C nucleation because they contained substrate screw dislocations. In contrast, under conditions of initial low nucleation rate on the step-free mesas, perfect 3C-SiC films (i.e., no observed defects) were reproducibly grown on mesas up to 0.4 mm by 0.4 mm in size.

[1] J. Powell, et. al. *Appl. Phys. Lett.*, vol. 77, no. 10, pp. 1449-1451, 2000.
[2] H. Matsunami, et. al. *Springer Proc. Physics,* vol. 34, pp. 34-39, 1989.

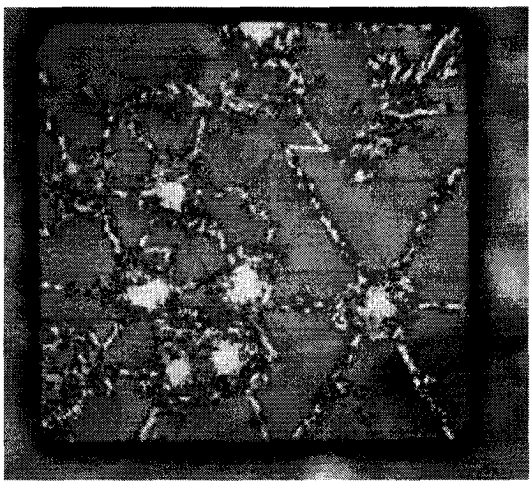

Fig. 1: Defective 3C-SiC heteroepitaxial layer with DPB's and SF's grown on a 0.2 mm x 0.2 mm 4H-SiC mesa that was not step-free because it contained screw dislocations.

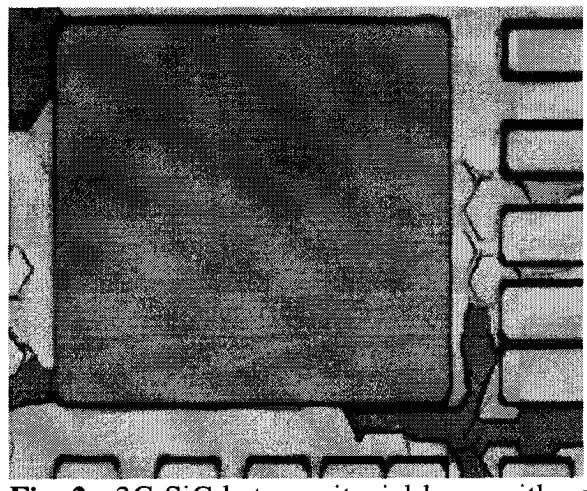

Fig. 2: 3C-SiC heteroepitaxial layer with no DPB's, and no SF's on a 0.3 mm x 0.3 mm 4H-SiC mesa. Both Fig. 1 & 2 oxidized to map polytype (dark = 3C) and defects.

AlGaN/GaN HETERO FIELD-EFFECT TRANSISTOR FOR A LARGE CURRENT OPERATION.

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GaN and related semiconductors are very promising for electric devices which can be used under high-power, high-frequency, and high-temperature conditions. Especially, it is expected that the on-state resistance of a GaN field-effect transistor (FET) is expected to be lower than that of Si or GaAs devices. However, there is no experimental report concerning the on-state resistance of a GaN-based FET. In this paper, it is reported for the first time that an AlGaN/GaN hetero FET (HFET) was operated above 20 A, and that the on-state resistance of the HFET is lower than that of a Si-based FET. A undoped $Al_{0.2}Ga_{0.8}N$(30nm)/GaN(2μm) heterostructure was grown on the sapphire substrate using a gas-source molecular beam epitaxy. The mobility of $Al_{0.2}Ga_{0.8}N$/GaN heterostructure was about 1200 cm^2/Vs at room temperature. We investigated the breakdown voltage of undoped GaN layer. The breakdown voltage of undoped GaN was over 2000 V (2 MV/cm). Before the formation of electrodes, Si-doped GaN with a carrier concentration of $5x10^{19}$ cm^{-3} was selectively grown in the source and drain regions in order to obtain a very low contact resistance.

After that, a large-size $Al_{0.2}Ga_{0.8}N$/GaN HFET was fabricated. The FET structure was formed using a dry-etching technique. The gate width was 20 cm and the gate length was 2 μm. The distance of source and drain was 6μm. The source and drain also had a multi-finger structure. The electrode materials of the source and the drain were Al/Ti/Au and the Schottky electrodes were Pt/Au. The distance between the source and drain was 6 μm. Multi-electrode structures were also fabricated using SiO_2 for isolating the source, drain, and gate electrodes, respectively. The HFET was operated at a current of over 20 A. The on-state resistance of the HFET was about 2 $m\Omega cm^2$. The transconductance (g_m) of this HFET was about 120 mS/mm. It was also confirmed that the breakdown voltage of schottky property was over 600 V. Therefore, a high power AlGaN/GaN HFET was thus demonstrated.